

## ReadMe file for Appendix B: Sample IBIS files

This directory contains the following files and their descriptions:

Ibischk4.exe

This is the IBIS Golden Parser version 4.1 (4/10/05) for checking files for errors. Run it from the DOS prompt line on the file by entering ">ibischk4.exe abcdefg.ibs > abcdefg\_results.txt" as an example. Always check the IBIS website for the latest version of the Parser:

<http://www.eda.org/pub/ibis/ibischk4/>

Download the version that will work with your operating system.

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abcdefg.ibs

This is a made-up, much shortened version of an IBIS file for a FPGA device for purposes of illustrating how the Golden Parser works.

gp1394c.ibs

This is TEXAS INSTRUMENTS' INCORPORATED Standard Linear and Logic IBIS Model of GTLP1394C. A 2-bit LVTTTL TO GTL+ ADJUSTABLE EDGE RATE BUS TRANSCIEVER with SELECTABLE POLARITY PKG SOIC,TVSOP and TSSOP. It is used with permission.

sn74ahct245.ibs

This is TEXAS INSTRUMENTS Inc's., Standard Linear and Logic Group's | IBIS Model of SN74AHCT245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS. This file contains package information for the following:

SSOP 20-pin (DB) package as [Component] AHCT245\_DB  
TVSOP 20-pin (DGV) package as [Component] AHCT245\_DGV  
SOIC 20-pin (DW) package as [Component] AHCT245\_DW  
PDIP 20-pin (N) package as [Component] AHCT245\_N  
TSSOP 20-pin (PW) package as [Component] AHCT245\_PW

This device can be powered at the following Vccs: 5 volt Vcc. This file provides unique models under the [Model Selector] for each Vcc. For operation at a specific Vcc, select the appropriate model after each [Model Selector] keyword. The file is used with permission.

virtex2.ibs

This is Xilinx's Virtex-II FPGA device. It is used with permission. Refer to the Xilinx subdirectory for additional information.

Cadence Macro Template

This is a sub directory with Cadence's pe\_2tap.dml Macro Template. It is used with permission.